



MOS 数据手册

NP4606H8A

30V Complementary MOS

Rev. 4.0

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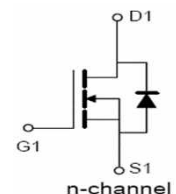
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NMOS 30V 5.5A/PMOS -30V -4.2A NP4606H8A

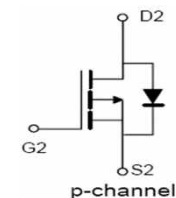
产品特性 Features

- ◆ 先进沟槽工艺技术 Advanced Trench Technology
- ◆ 超低栅极电荷 Super Low Gate Charge
- ◆ 超低 Ron 高密度单元设计 High Density Cell Design for Ultra Low Rdson
- ◆ RoHS 产品 RoHS Product

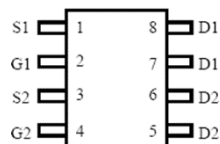


应用领域 Applications

- ◆ 负载开关 Load Switching
- ◆ 脉宽调制器 PWM
- ◆ DC/DC 转换器 DC/DC Converter
- ◆ 高频开关 High Frequency Switching



关键参数与封装信息 Key Performance and Package Parameters



SOP8

产品型号 Part No.	封装 Package	漏极-源极电压 V _{DS}	漏极电流 I _D	导通电阻 R _{DS(on) Typ.}	印记 Marking
NP4606H8A	SOP8	30V	5.5A	16.5mΩ @ V _{GS} =10V	NP4606H8A
		-30V	-4.2A	36.5mΩ @ V _{GS} =-10V	

最大额定值 Maximum Ratings

参数 Parameter	符号 Symbol	数值 NMOS	数值 PMOS	单位 Unit
最高漏极-源极直流电压 Drain to Source Voltage	V _{DS}	30	-30	V
最高栅源电压 Gate to Source Voltage	V _{GS}	±20	±20	V
连续漏极电流 Drain Current-Continuous, Limited by T _{vjmax} TC = 25°C TC = 100°C	I _D	5.5 3.5	-4.2 -2.7	A
最大脉冲漏极电流 Pulse Drain Current ^① PW=5μs, Duty Cycle≤2%	I _{Dpuls}	30	-30	A
二极管正向电流 Diode Forward Current, Limited by T _{vjmax} TC = 25°C	I _S /I _{SM}	5.5/30	-4.2/-30	A
单脉冲雪崩能量 Single Pulsed Avalanche Energy ^②	E _{AS}	6.25	6.25	mJ
最大耗散功率 Maximum Power Dissipation TC = 25°C TC = 100°C	P _D	2 0.8	2 0.8	W
结温 Operating Junction Temperature	T _J	-55...+150	-55...+150	°C
存储温度 Storage Temperature	T _{stg}	-55...+150	-55...+150	°C
最高焊接温度 Maximum Soldering Temperature		260	260	°C

① 脉冲宽度由最高结温限制 Pulse width limited by maximum junction temperature

② EAS 测试条件(T_J=25°C): NMOS: V_{DD}=20V, I_{AR}=5A, L=0.5mH, R_g=25Ω/ PMOS: V_{DD}=-20V, I_{AR}=-5A, L=0.5mH, R_g=25Ω

热阻特性 Thermal Resistance

参数 Parameter	符号 Symbol	数值 (最大) Max. Value	单位 Unit
结到环境热阻 Thermal Resistance Junction to Ambient ^③	R _{θJA}	63.2	°C /W

③ Device on 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one layer, 7μm thick) copper area for drain connection. PCB is vertical in still air.

NMOS 电气特性 Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

项目 Parameter	符号 Symbol	测试条件 Conditions	数值 Value			单位 Unit
			Min.	Typ.	Max.	
漏-源击穿电压 Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
零栅压下漏极漏电流 Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$ $T_J=25^\circ\text{C}$ $T_J=150^\circ\text{C}$	-	-	1 100	μA
栅极漏电流 Gate to Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
阈值电压 Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.2	V
静态导通电阻 Drain to Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4A$	-	16.5	21.4	$m\Omega$
		$V_{GS}=4.5V, I_D=3A$	-	23.5	32.9	$m\Omega$
正向压降 Diode Forward Voltage	V_{SD}	$I_S=4A, V_{GS}=0V$	-	-	1.2	V
输入电容 Input Capacitance	C_{iss}	$V_{DS}=15V$ $V_{GS}=0V$ $f=1\text{MHz}$	-	457	-	pF
输出电容 Output Capacitance	C_{oss}		-	74.1	-	pF
反向传输电容 Reverse Transfer Capacitance	C_{rss}		-	62.9	-	pF
栅极电荷总量 Total Gate Charge	Q_g	$V_{DS}=15V$ $V_{GS}=10V$ $I_{DS}=1A$	-	9.89	-	nC
栅极-源极电荷 Gate to Source Charge	Q_{gs}		-	0.87	-	
栅极-漏极电荷 Gate to Drain Charge	Q_{gd}		-	2.29	-	
开启延迟时间 Turn-On Delay Time	$t_{d(on)}$	$T_J=25^\circ\text{C}$ $V_{DD}=15V, I_D=3A$ $V_{GS}=10V, R_G=3\Omega$	-	10	-	ns
上升时间 Rise Time	t_r		-	14	-	
关断延迟时间 Turn-Off Delay Time	$t_{d(off)}$		-	32	-	
下降时间 Fall Time	t_f		-	6	-	
反向恢复时间 Reverse Recovery Time	t_{rr}	$I_F=3A, di/dt=100A/\mu s$	-	12	-	ns
反向恢复电荷 Reverse Recovery Charge	Q_{rr}		-	3	-	nC

NMOS 特征曲线 Characteristic Curve

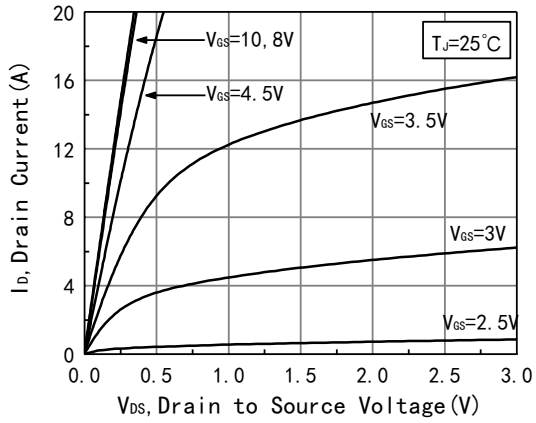


Figure 1. Typical Output Characteristics

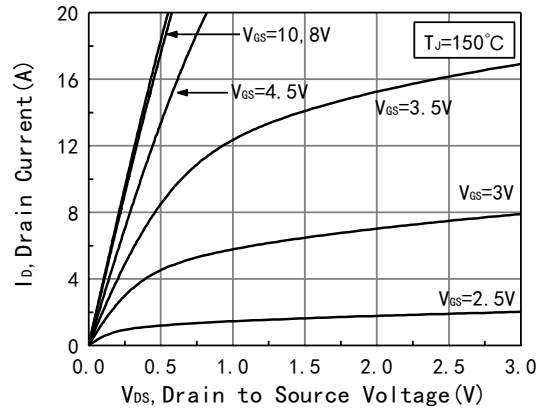


Figure 2. Typical Output Characteristics

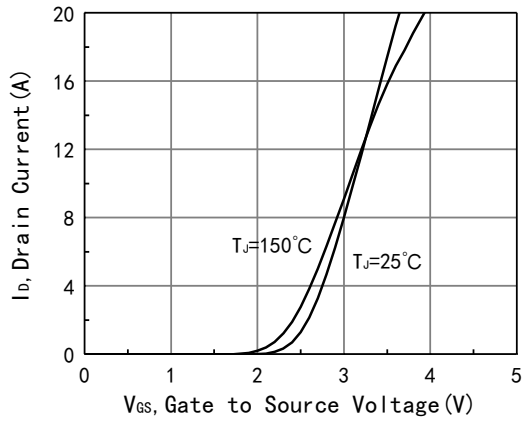


Figure 3. Typical Transfer Characteristics

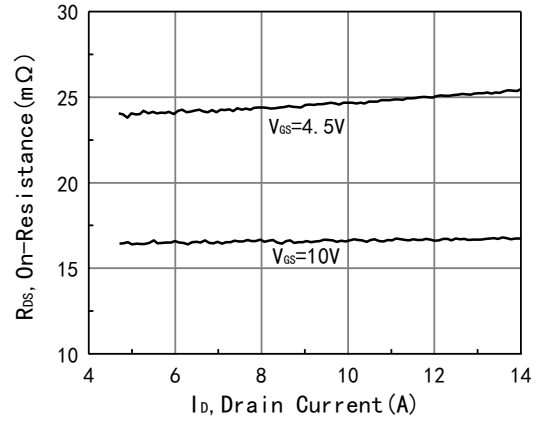


Figure 4. $R_{DS(on)}$ vs. I_D

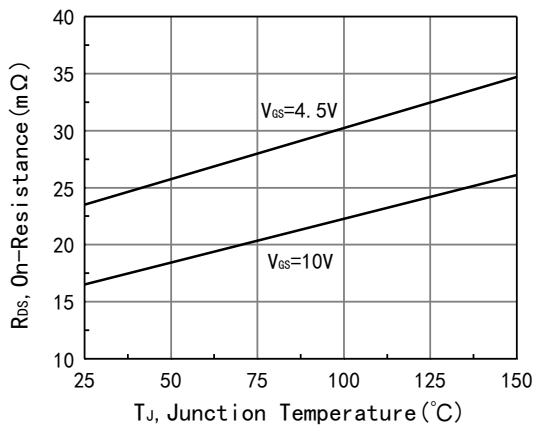


Figure 5. $R_{DS(on)}$ vs. T_J

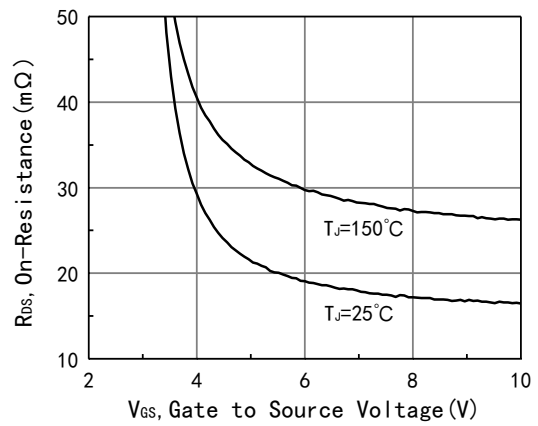


Figure 6. $R_{DS(on)}$ vs. V_{GS}

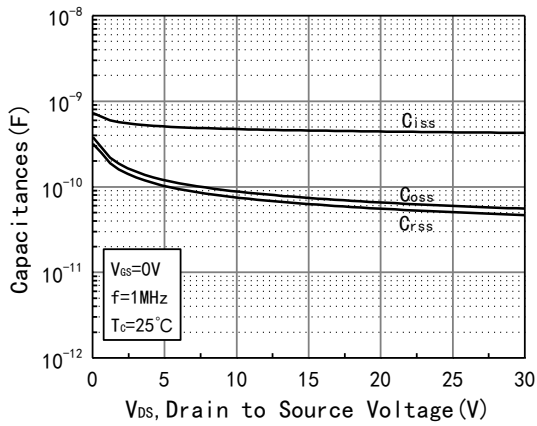


Figure 7. Capacitance vs. Vds

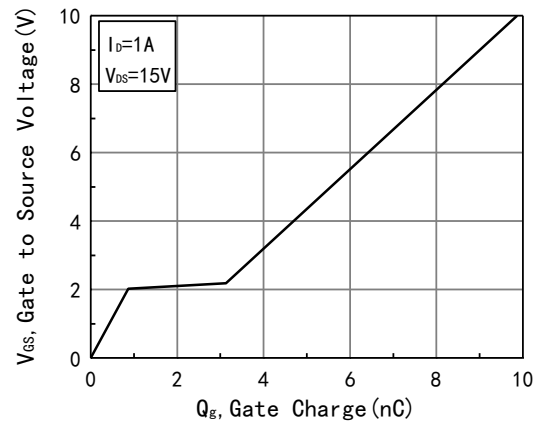


Figure 8. Gate Charge Characteristic

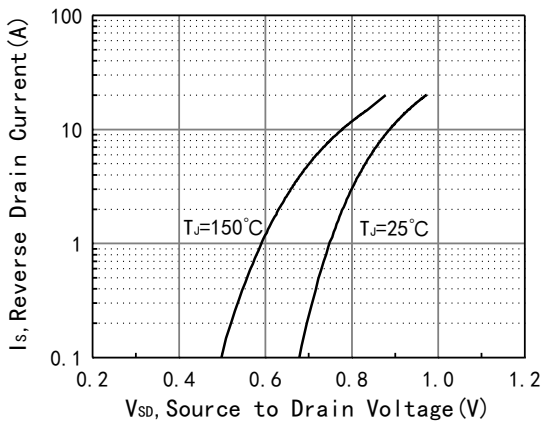


Figure 9. Diode Forward Characteristic

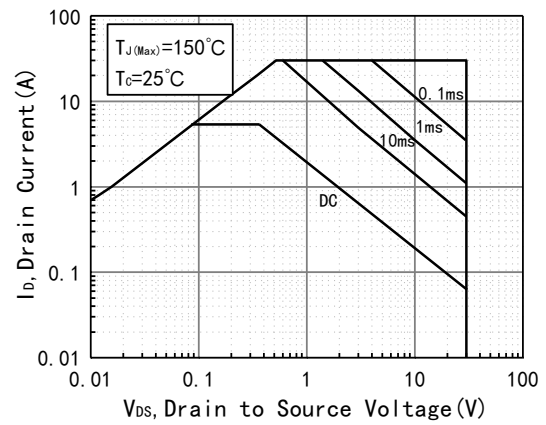


Figure 10. Safe Operating Area

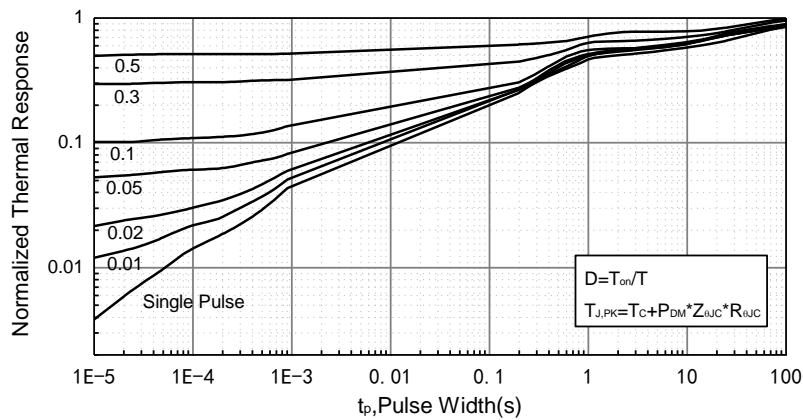


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu s$, Pulse Delay $\leq 200\mu s$.

PMOS 电气特性 Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

项目 Parameter	符号 Symbol	测试条件 Conditions	数值 Value			单位 Unit
			Min.	Typ.	Max.	
漏-源击穿电压 Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
零栅压下漏极漏电流 Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$ $T_J=25^\circ\text{C}$ $T_J=150^\circ\text{C}$	-	-	-1 -100	μA
栅极漏电流 Gate to Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
阈值电压 Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-2.2	V
静态导通电阻 Drain to Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4A$	-	36.5	47	$m\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	-	52	72	$m\Omega$
正向压降 Diode Forward Voltage	V_{SD}	$I_S=-4A, V_{GS}=0V$	-	-	-1.2	V
输入电容 Input Capacitance	C_{iss}	$V_{DS}=-15V$ $V_{GS}=0V$ $f=1\text{MHz}$	-	552	-	pF
输出电容 Output Capacitance	C_{oss}		-	84.5	-	pF
反向传输电容 Reverse Transfer Capacitance	C_{rss}		-	74.8	-	pF
栅极电荷总量 Total Gate Charge	Q_g	$V_{DS}=-15V$ $V_{GS}=-10V$ $I_{DS}=-1A$	-	11.2	-	nC
栅极-源极电荷 Gate to Source Charge	Q_{gs}		-	2.5	-	
栅极-漏极电荷 Gate to Drain Charge	Q_{gd}		-	2.9	-	
开启延迟时间 Turn-On Delay Time	$t_{d(on)}$	$T_J=25^\circ\text{C}$ $V_{DD}=-15V, I_D=-3A$ $V_{GS}=-10V, R_G=3\Omega$	-	9.5	-	ns
上升时间 Rise Time	t_r		-	5.4	-	
关断延迟时间 Turn-Off Delay Time	$t_{d(off)}$		-	42.5	-	
下降时间 Fall Time	t_f		-	13.6	-	
反向恢复时间 Reverse Recovery Time	t_{rr}	$I_F=-3A, di/dt=100A/\mu s$	-	12	-	ns
反向恢复电荷 Reverse Recovery Charge	Q_{rr}		-	3	-	nC

PMOS 特征曲线 Characteristic Curve

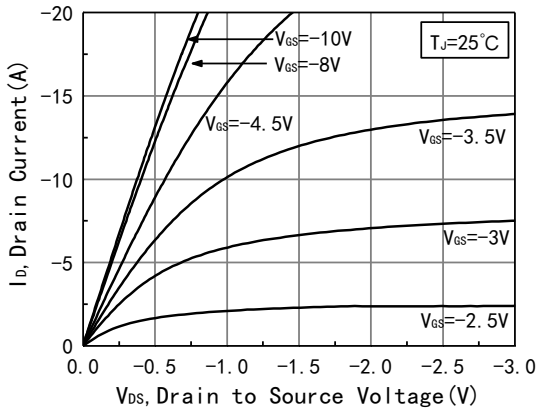


Figure 1. Typical Output Characteristics

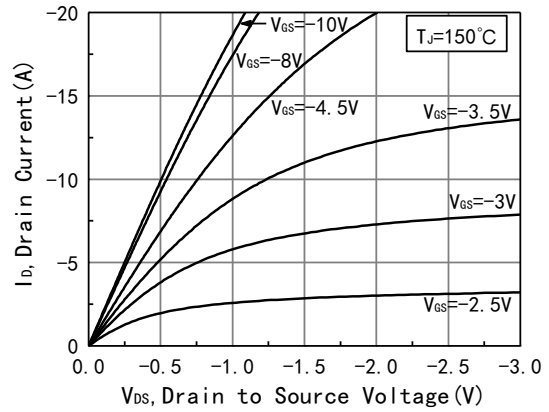


Figure 2. Typical Output Characteristics

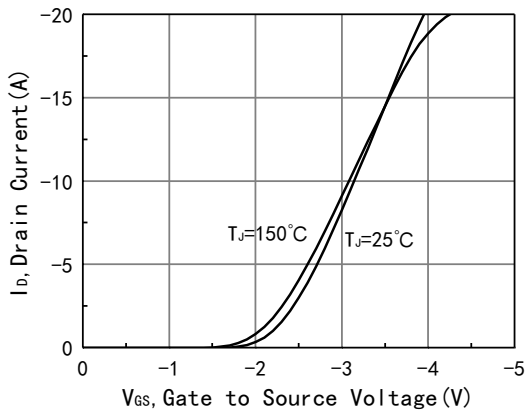


Figure 3. Typical Transfer Characteristics

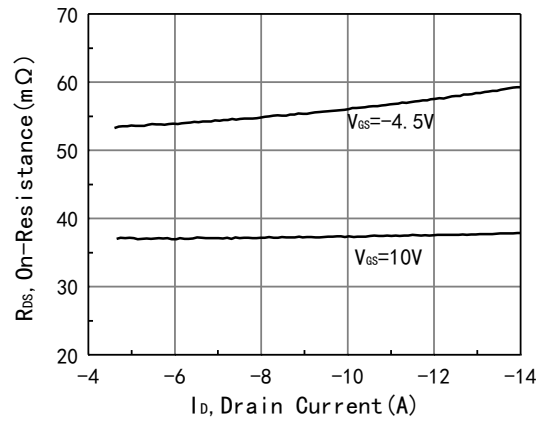


Figure 4. $R_{DS(on)}$ vs. I_D

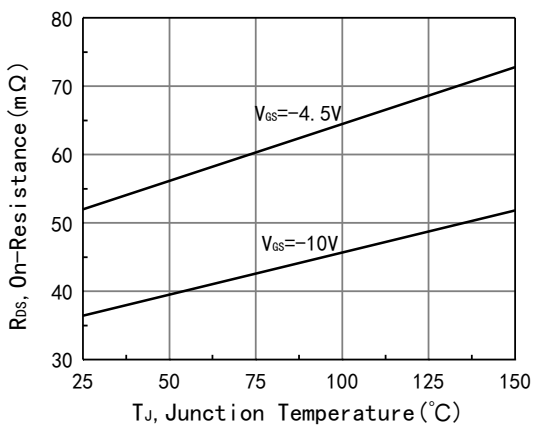


Figure 5. $R_{DS(on)}$ vs. T_J

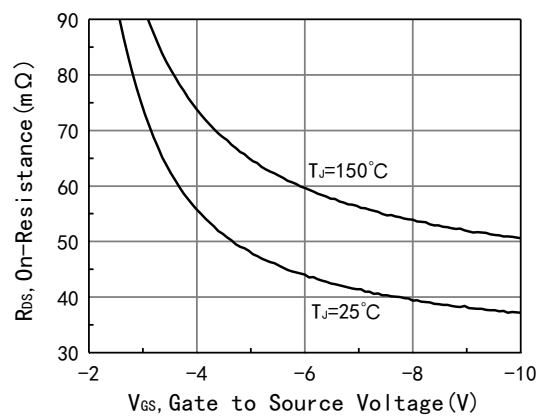


Figure 6. $R_{DS(on)}$ vs. V_{GS}

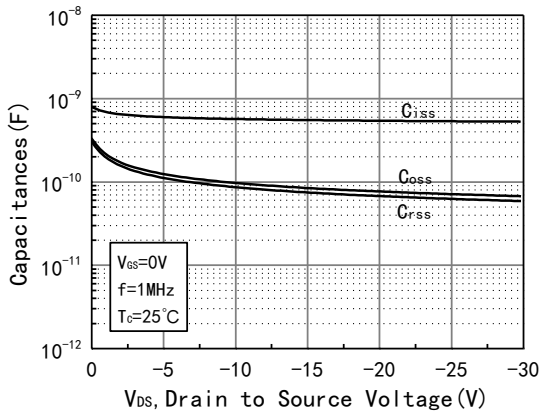


Figure 7. Capacitance vs. Vds

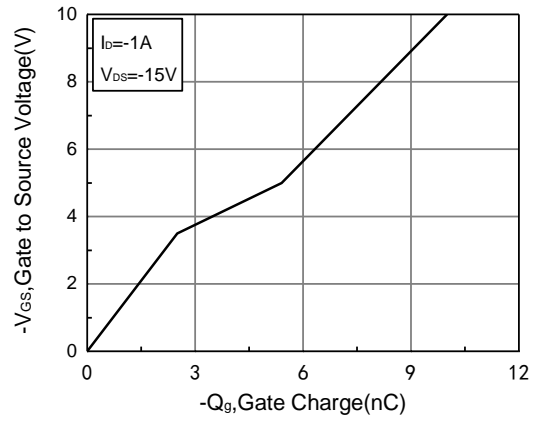


Figure 8. Gate Charge Characteristic

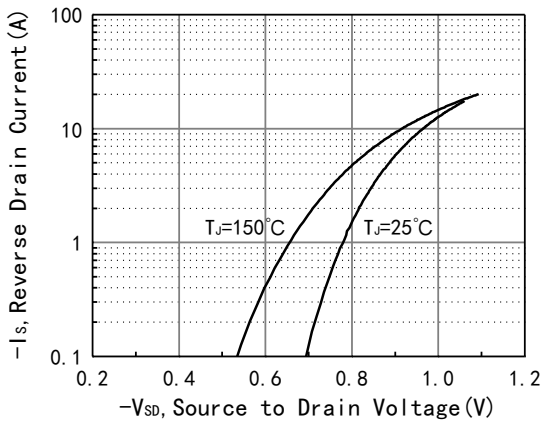


Figure 9. Diode Forward Characteristic

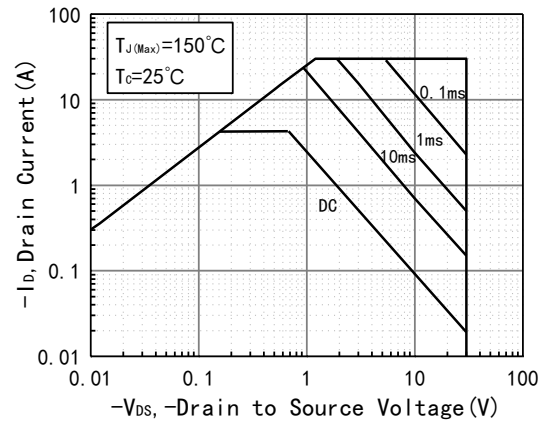


Figure 10. Safe Operating Area

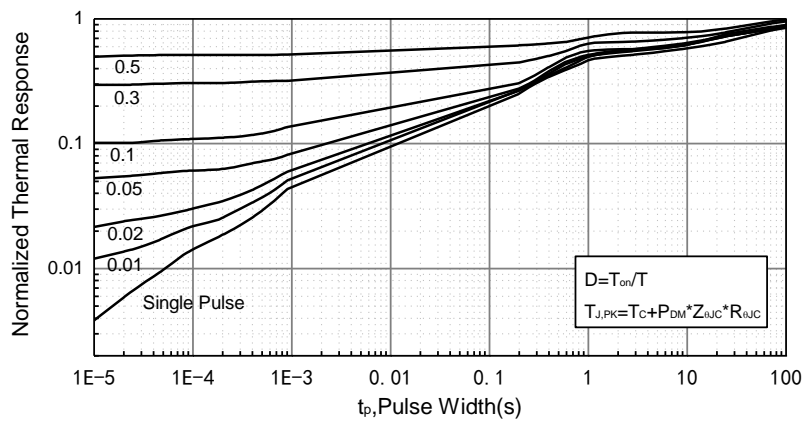
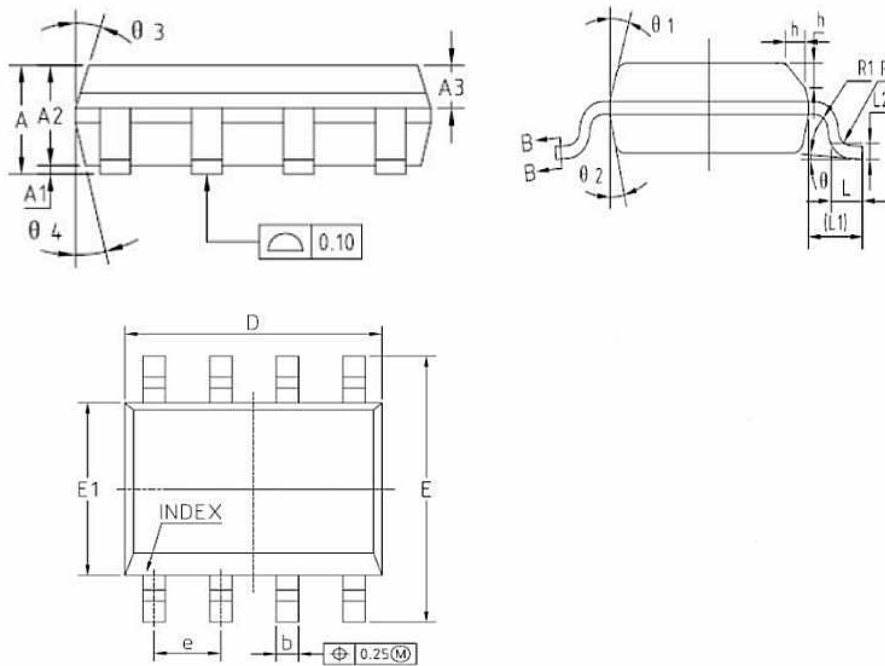


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu s$, Pulse Delay $\leq 200\mu s$.

外形尺寸 Mechanical Data: SOP8



Dimensions In Millimeters			
Symbol	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.10	0.15	0.20
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	-	0.51
D	4.85	4.90	4.95
E	5.85	6.00	6.15
E1	3.85	3.90	3.95
e	1.245	1.27	1.295
L	0.45	0.60	0.75
L1	-	1.040REF	-
L2	-	0.250BSC	-
$\theta 1-4$	12°REF		
h	0.40REF		
R	0.15°REF		
R1	0.15°REF		

历史版本

版本号	时间	修改内容
V1.0	2019 年 3 月	初始版本
V2.0	2020 年 1 月	部分 SPEC 收紧
V3.0	2020 年 9 月	模板更新
V4.0	2022 年 10 月	更新参数及曲线