



NMOS 数据手册

NPM4614PD6A

40V Complementary MOS

Rev. 1.0

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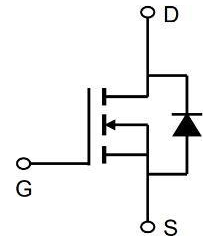
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NMOS 40V/20A/PMOS -40V/-20A NPM4614PD6A

产品特性 Features

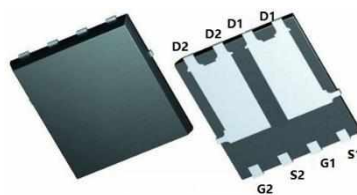
- ◆ 先进沟槽工艺技术 Advanced Trench Technology
- ◆ 超低栅极电荷 Super Low Gate Charge
- ◆ 超低 Ron 高密度单元设计 High Density Cell Design for Ultra Low Rdson
- ◆ RoHS 产品 RoHS Product



应用领域 Applications

- ◆ 负载开关 Load Switching
- ◆ 脉宽调制器 PWM
- ◆ DC/DC 转换器 DC/DC Converter
- ◆ 高频开关 High Frequency Switching

关键参数与封装信息 Key Performance and Package Parameters



PDFN5x6

产品型号 Part No.	封装 Package	漏极-源极电压 V _{DS}	漏极电流 I _D	导通电阻 R _{DS(on)} Typ.
NPM4614PD6A	PDFN5x6	40V	20A	14.5mΩ @ V _{GS} =10V
		-40V	-20A	27mΩ @ V _{GS} =-10V

最大额定值 Maximum Ratings

参数 Parameter	符号 Symbol	数值 NMOS	数值 PMOS	单位 Unit
最高漏极-源极直流电压 Drain to Source Voltage	V _{DS}	40	-40	V
最高栅源电压 Gate to Source Voltage	V _{GS}	±20	±20	V
连续漏极电流 Drain Current-Continuous, Limited by T _{vjmax} TC = 25°C TC = 100°C	I _D	20 12.5	-20 -12.5	A
最大脉冲漏极电流 Pulse Drain Current ^① PW≤300μs,Duty Cycle≤2%	I _{Dpuls}	40	-40	A
二极管正向电流 Diode Forward Current, Limited by T _{vjmax} TC = 25°C	I _S /I _{SM}	20/40	-20/-40	A
单脉冲雪崩能量 Single Pulsed Avalanche Energy ^②	E _{AS}	16	25	mJ
最大耗散功率 Maximum Power Dissipation TC = 25°C TC = 100°C	P _D	24 9.6	24 9.6	W
结温 Operating Junction Temperature	T _J	-55...+150	-55...+150	°C
存储温度 Storage Temperature	T _{stg}	-55...+150	-55...+150	°C
最高焊接温度 Maximum Soldering Temperature		260	260	°C

① 脉冲宽度由最高结温限制 Pulse width limited by maximum junction temperature

② EAS 测试条件(T_J=25°C): NMOS: V_{DD}=20V, I_{AR}=8A, L=0.5mH, R_g=25Ω/ PMOS: V_{DD}=-20V, I_{AR}=-10A, L=0.5mH, R_g=25Ω

热阻特性 Thermal Resistance

参数 Parameter	符号 Symbol	数值 (最大) Max. Value	单位 Unit
结到管壳热阻 Thermal Resistance Junction to Case	R _{θJC}	5.2	°C/W
结到环境热阻 Thermal Resistance Junction to Ambient ^③	R _{θJA}	50	°C/W

③ Device on 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one layer, 7μm thick) copper area for drain connection. PCB is vertical in still air.

NMOS 电气特性 Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

项目 Parameter	符号 Symbol	测试条件 Conditions	数值 Value			单位 Unit
			Min.	Typ.	Max.	
漏-源击穿电压 Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
零栅压下漏极漏电流 Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$ $T_J=25^\circ\text{C}$ $T_J=150^\circ\text{C}$	-	-	1 100	μA
栅极漏电流 Gate to Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
阈值电压 Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.2	V
静态导通电阻 Drain to Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	14.5	18.5	$m\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	20	28	$m\Omega$
正向压降 Diode Forward Voltage	V_{SD}	$I_S=4A, V_{GS}=0V$	-	0.8	1.2	V
输入电容 Input Capacitance	C_{iss}	$V_{DS}=20V$ $V_{GS}=0V$ $f=1\text{MHz}$	-	927	-	pF
输出电容 Output Capacitance	C_{oss}		-	74	-	pF
反向传输电容 Reverse Transfer Capacitance	C_{rss}		-	64.7	-	pF
栅极电荷总量 Total Gate Charge	Q_g	$V_{DS}=20V$ $V_{GS}=10V$ $I_{DS}=10A$	-	20.1	-	nC
栅极-源极电荷 Gate to Source Charge	Q_{gs}		-	2.39	-	
栅极-漏极电荷 Gate to Drain Charge	Q_{gd}		-	5.57	-	
开启延迟时间 Turn-On Delay Time	$t_{d(on)}$	$T_J=25^\circ\text{C}$ $V_{DD}=20V, I_D=10A$ $V_{GS}=10V, R_G=3\Omega$	-	9	-	ns
上升时间 Rise Time	t_r		-	10	-	
关断延迟时间 Turn-Off Delay Time	$t_{d(off)}$		-	34	-	
下降时间 Fall Time	t_f		-	6	-	
反向恢复时间 Reverse Recovery Time	t_{rr}	$I_F=10A, di/dt=150A/\mu s$	-	16	-	ns
反向恢复电荷 Reverse Recovery Charge	Q_{rr}		-	9	-	nC

NMOS 特征曲线 Characteristic Curve

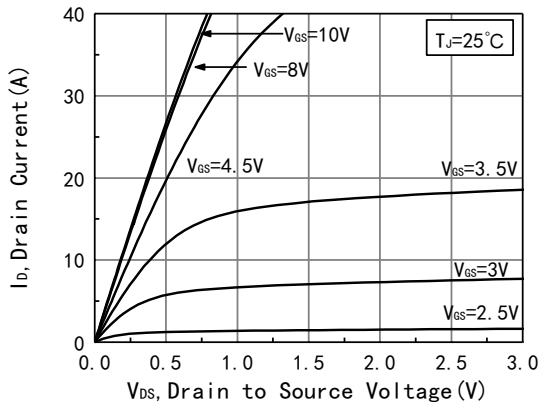


Figure 1. Typical Output Characteristics

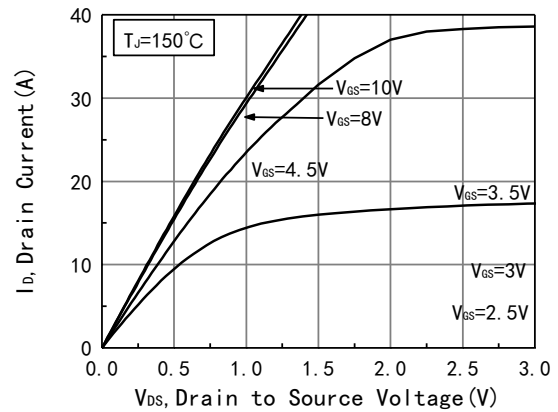


Figure 2. Typical Output Characteristics

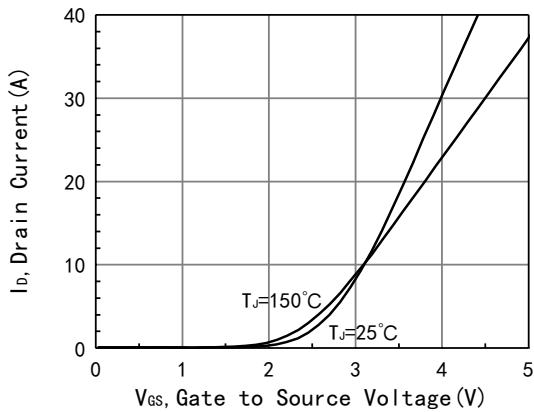


Figure 3. Typical Transfer Characteristics

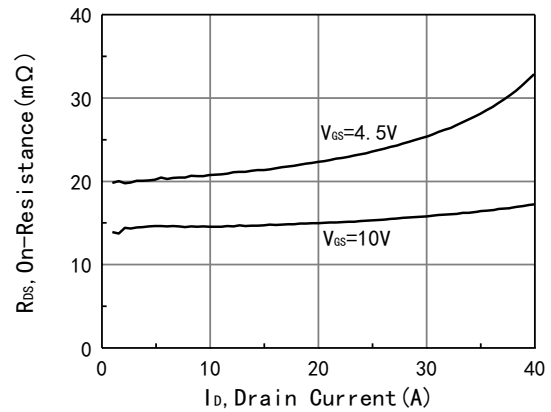


Figure 4. $R_{DS(on)}$ vs. I_D

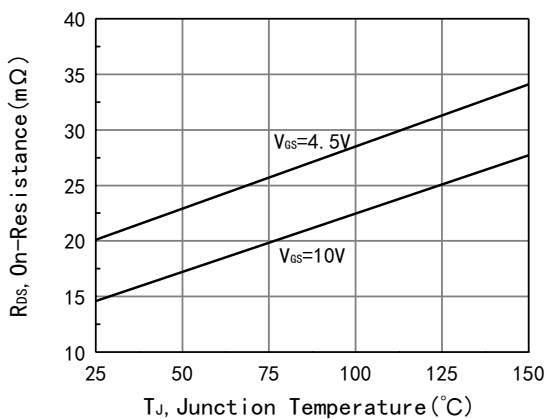


Figure 5. $R_{DS(on)}$ vs. T_J

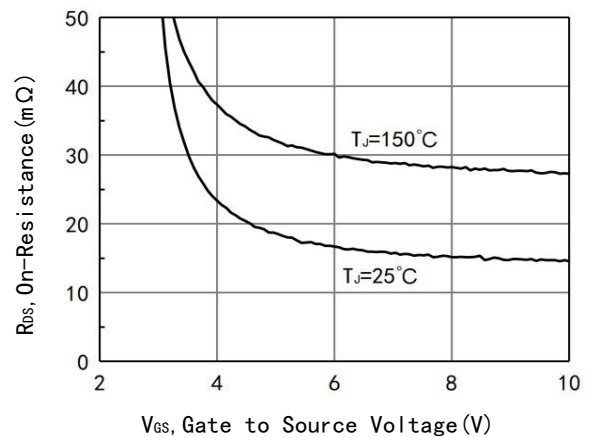


Figure 6. $R_{DS(on)}$ vs. V_{GS}

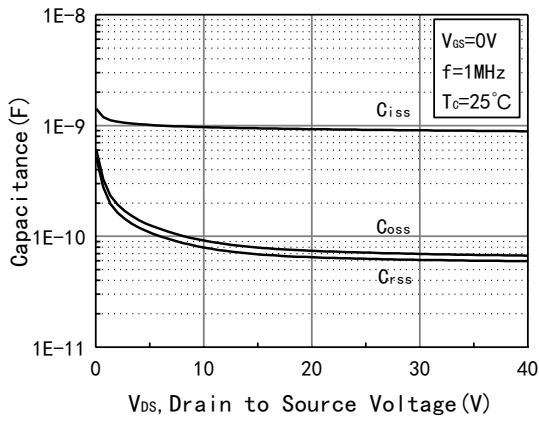


Figure 7. Capacitance vs. Vds

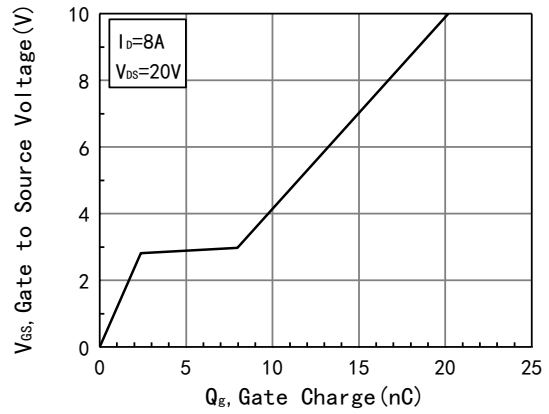


Figure 8. Gate Charge Characteristic

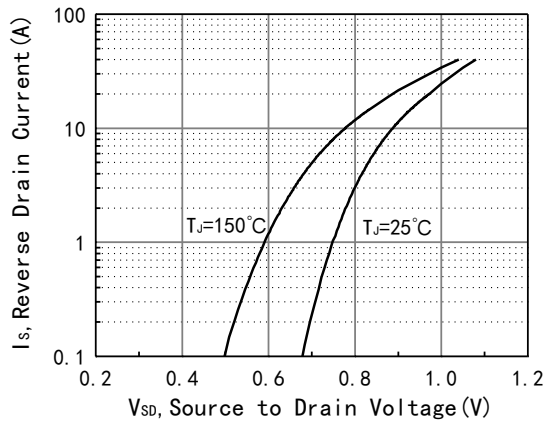


Figure 9. Diode Forward Characteristic

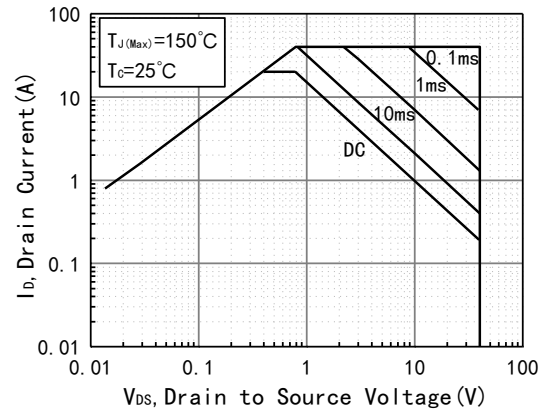


Figure 10. Safe Operating Area

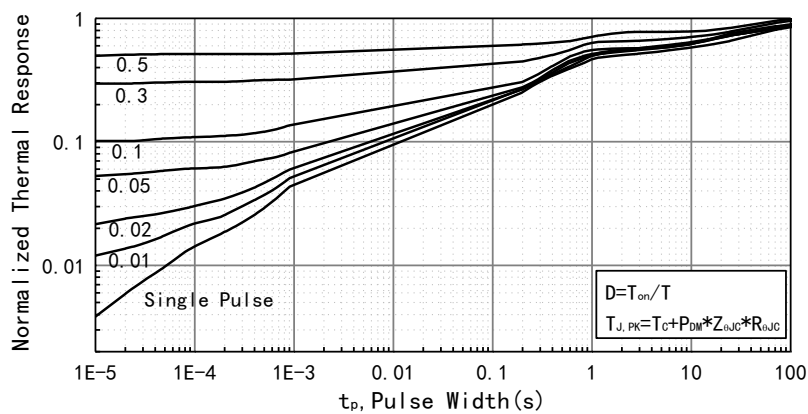


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu\text{s}$, Pulse Delay $\leq 200\mu\text{s}$.

PMOS 电气特性 Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

项目 Parameter	符号 Symbol	测试条件 Conditions	数值 Value			单位 Unit
			Min.	Typ.	Max.	
漏-源击穿电压 Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
零栅压下漏极漏电流 Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$ $T_J=25^\circ\text{C}$ $T_J=150^\circ\text{C}$	-	-	-1 -100	μA
栅极漏电流 Gate to Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
阈值电压 Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-2.2	V
静态导通电阻 Drain to Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$	-	27	35	$m\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	-	33	45	$m\Omega$
正向压降 Diode Forward Voltage	V_{SD}	$I_S=-4A, V_{GS}=0V$	-	-0.8	-1.2	V
输入电容 Input Capacitance	C_{iss}	$V_{DS}=-20V$ $V_{GS}=0V$ $f=1\text{MHz}$	-	1286	-	pF
输出电容 Output Capacitance	C_{oss}		-	107	-	pF
反向传输电容 Reverse Transfer Capacitance	C_{rss}		-	98	-	pF
栅极电荷总量 Total Gate Charge	Q_g	$V_{DS}=-20V$ $V_{GS}=-10V$ $I_{DS}=-10A$	-	23.4	-	nC
栅极-源极电荷 Gate to Source Charge	Q_{gs}		-	3.1	-	
栅极-漏极电荷 Gate to Drain Charge	Q_{gd}		-	2.8	-	
开启延迟时间 Turn-On Delay Time	$t_{d(on)}$	$T_J=25^\circ\text{C}$ $V_{DD}=-20V, I_D=-10A$ $V_{GS}=-10V, R_G=3.3\Omega$	-	10	-	ns
上升时间 Rise Time	t_r		-	8	-	
关断延迟时间 Turn-Off Delay Time	$t_{d(off)}$		-	24	-	
下降时间 Fall Time	t_f		-	9	-	
反向恢复时间 Reverse Recovery Time	t_{rr}	$I_F=-10A, di/dt=150A/\mu s$	-	21	-	ns
反向恢复电荷 Reverse Recovery Charge	Q_{rr}		-	11	-	nC

PMOS 特征曲线 Characteristic Curve

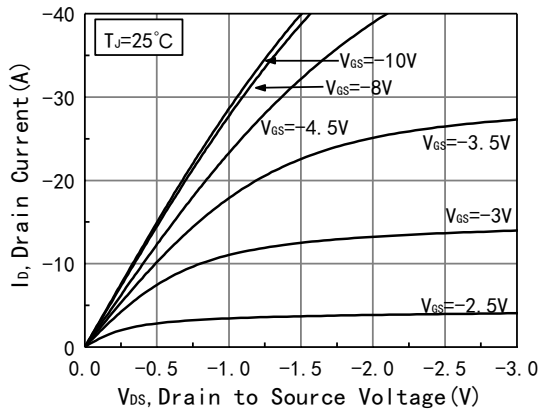


Figure 1. Typical Output Characteristics

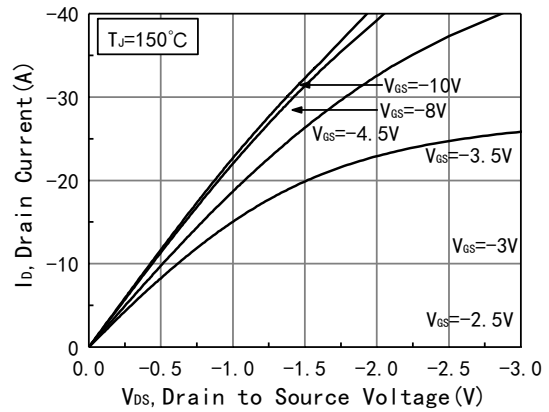


Figure 2. Typical Output Characteristics

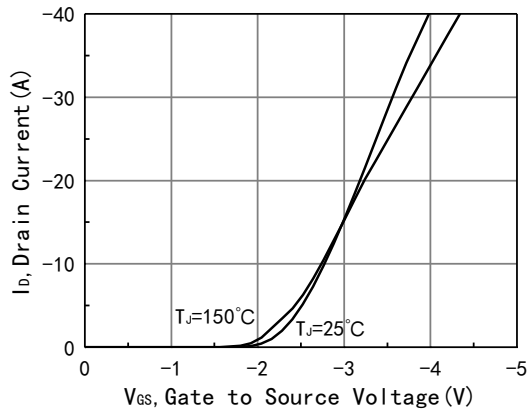


Figure 3. Typical Transfer Characteristics

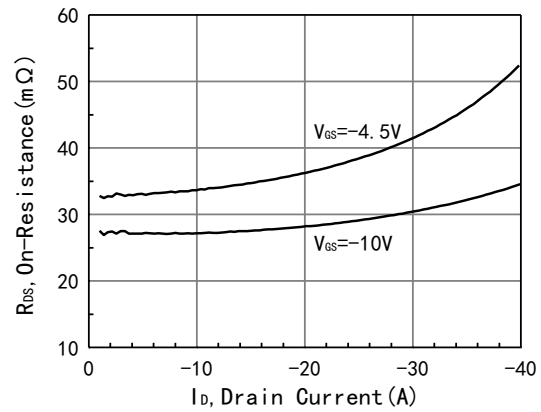


Figure 4. $R_{DS(on)}$ vs. I_D

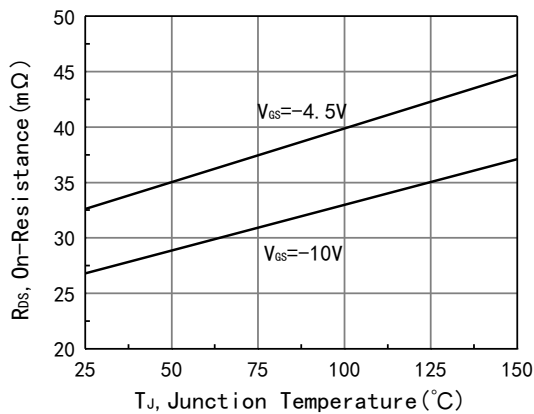


Figure 5. $R_{DS(on)}$ vs. T_J

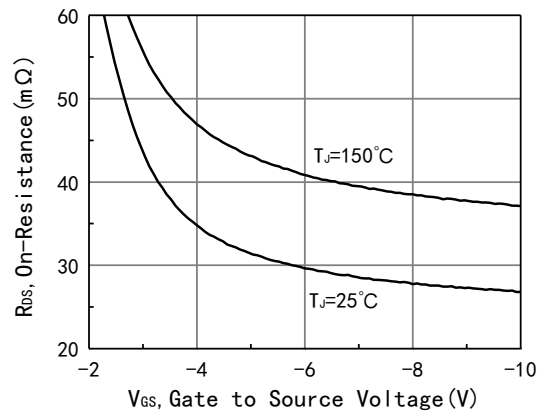


Figure 6. $R_{DS(on)}$ vs. V_{GS}

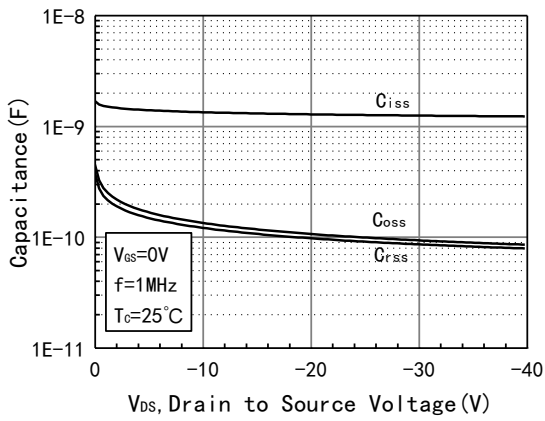


Figure 7. Capacitance vs. Vds

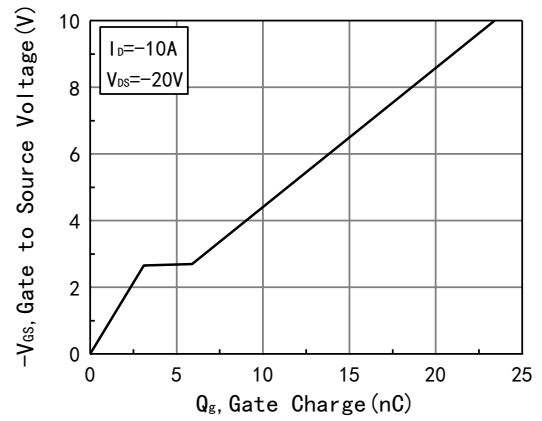


Figure 8. Gate Charge Characteristic

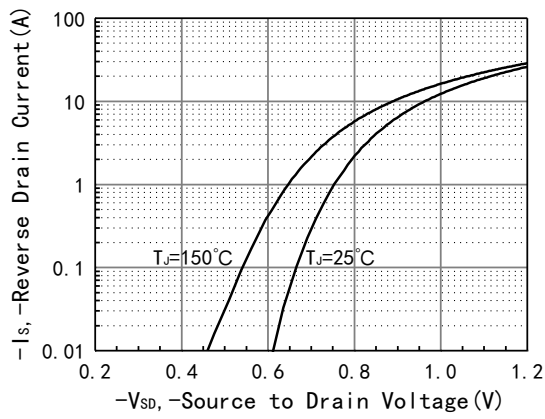


Figure 9. Diode Forward Characteristic

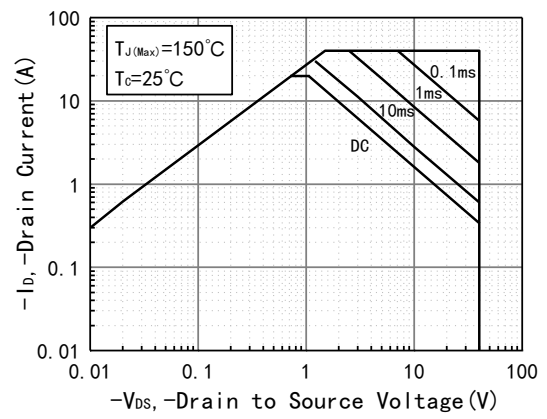


Figure 10. Safe Operating Area

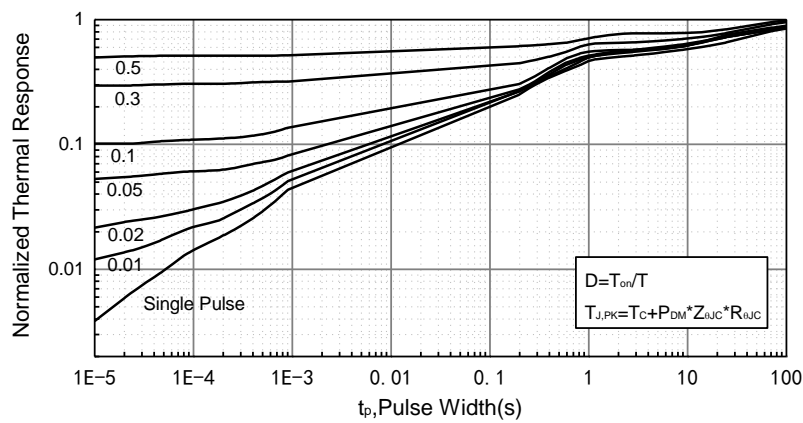
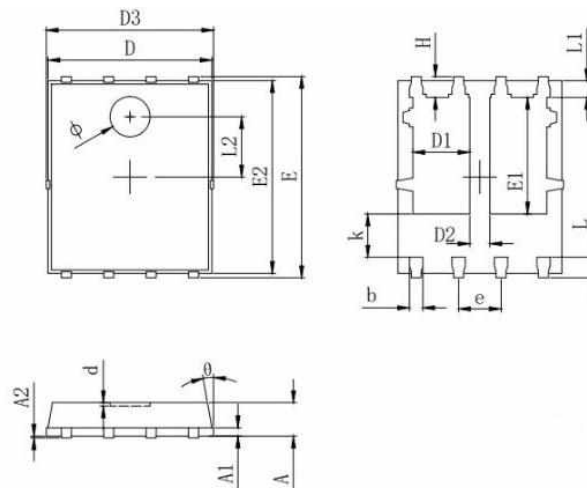


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu s$, Pulse Delay $\leq 200\mu s$.

外形尺寸 Mechanical Data: PFN5*6



Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	1.605	1.705	1.805
D2	0.500	0.600	0.700
D3	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
Φ	1.100	1.200	1.300
d			0.100

历史版本

版本号	时间	修改内容
V1.0	2023 年 2 月	初始版本